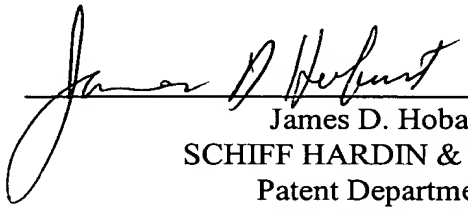
REMARKS

Claims 1-6 are presented for examination.

By this amendment, the translation of the original PCT Application has been amended to correct grammatical errors and to provide headings. These corrections are in the Substitute Specification, which contains no new matter, and the changes are shown in the marked-up version attached as an appendix. In addition, a new Abstract has been submitted and is attached herewith, with the changes in the Abstract being shown in the marked-up version attached as the appendix. Finally, claims 1-6 have been amended to remove the reference numerals and to place them in form for examination in the United States Patent Office. These amendments are shown in the appendix, with insertions being underlined and with portions being removed in brackets. It is submitted that the amendments to claims 1-6 do not change the indication of allowable subject matter set forth in the Preliminary Examination Report dated August 21, 2001.

Respectfully submitted,



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DATED: November 15, 2001

FIG 1

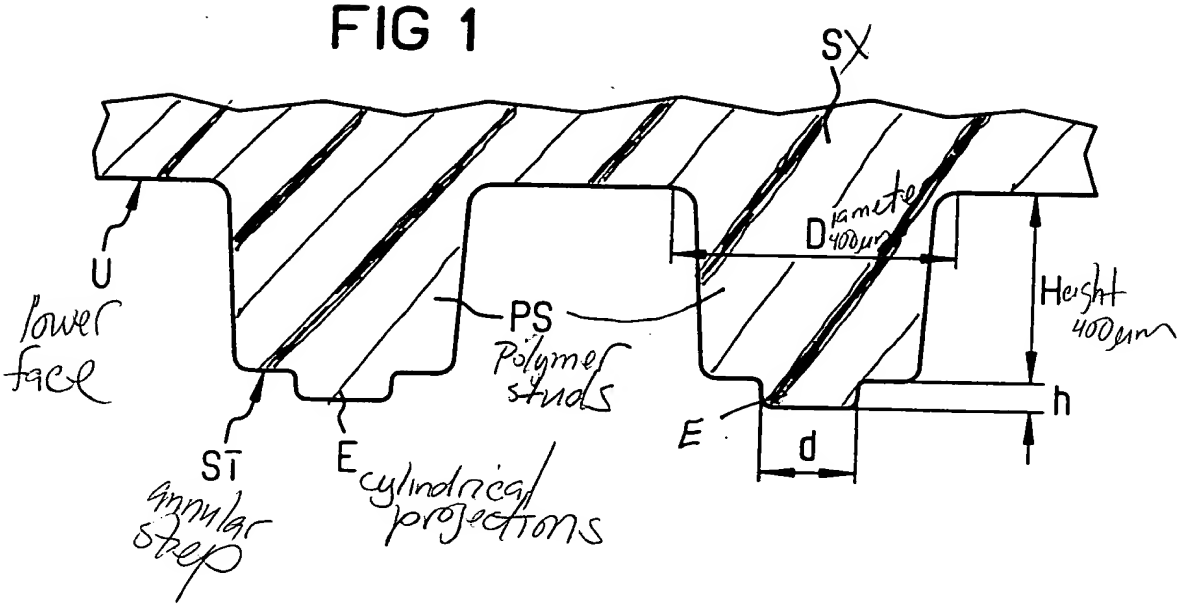


FIG 2

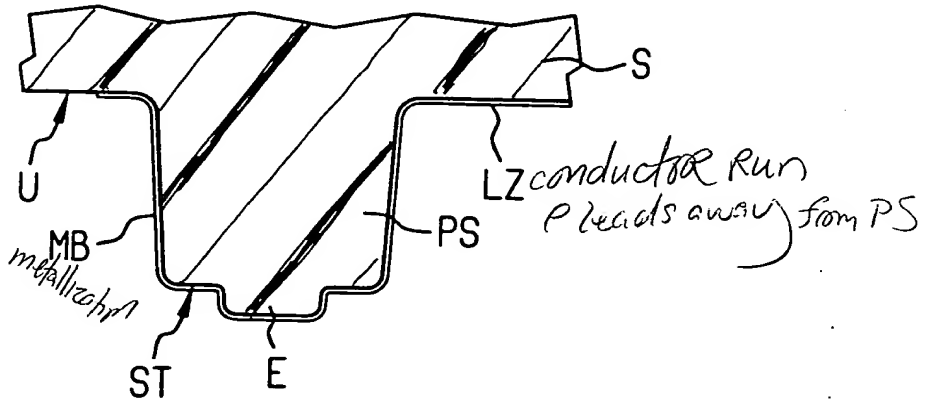


FIG 3

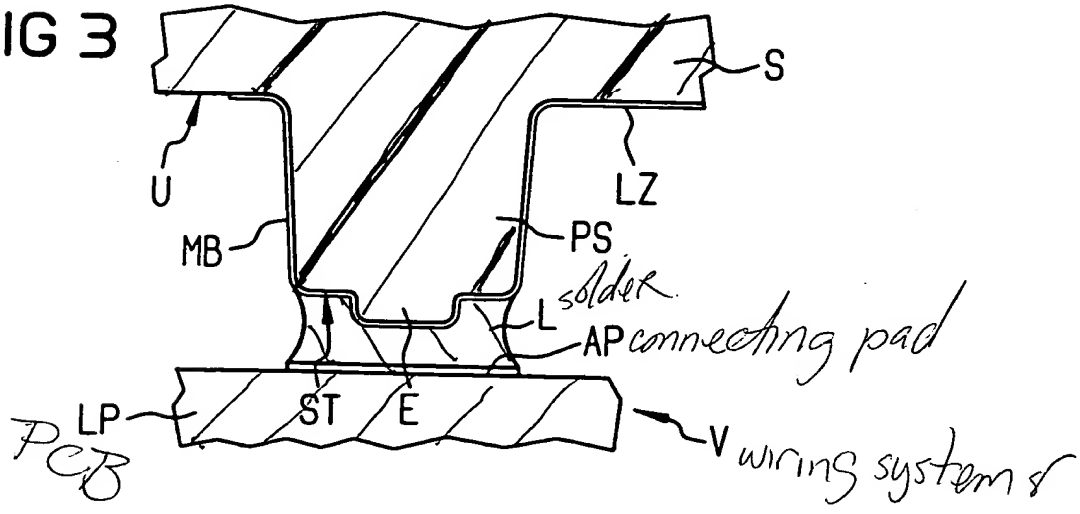


FIG 4

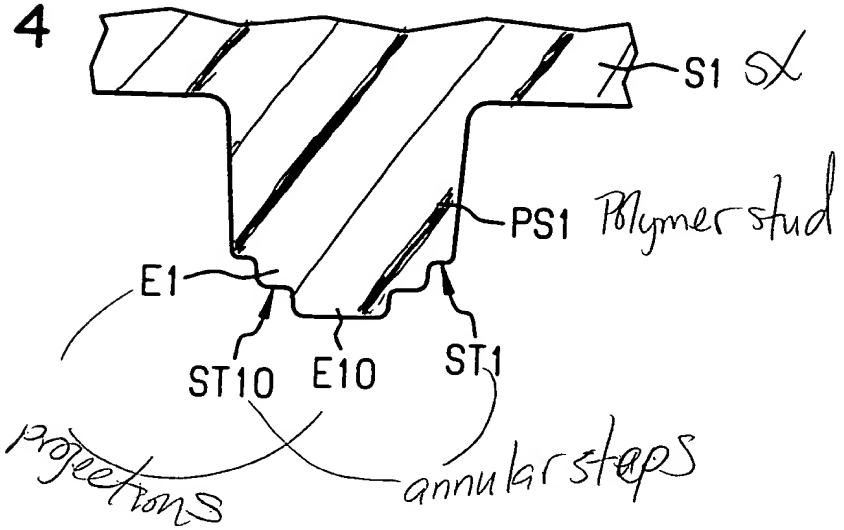


FIG 5

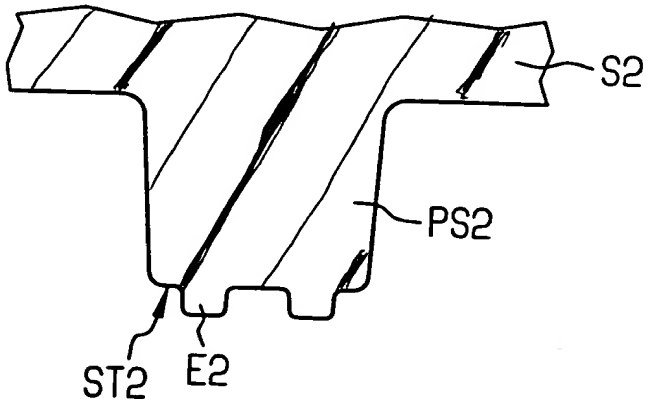
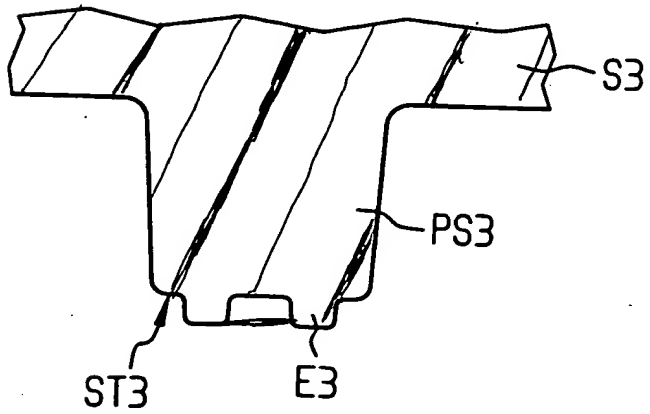


FIG 6



Appendix

~~Description~~ Title

Substrate ~~having~~ with at least two metallized polymer studs for soldered connections to a wiring

Background of the Invention

Integrated circuits are having ever greater numbers of connections, and are at the same time being ~~ever~~ even further miniaturized. The difficulties expected with this increase in miniaturisation with the application of solder paste and component placement are intended to be overcome by new package forms with either single-chip modules, few-chip modules or multi-chip modules preferably in a ball grid array package ~~being preferred, in particular, in this case~~ (see German periodical ~~IEEE~~ productronic VDE 5, 1994, pages 54, 55). These modules are based on a plated-through substrate, on which contact is made with the chips, for example, via contact-making wires or by means of flipchip mounting. On the lower face of the substrate, there is a ball grid array (BGA), which is frequently also referred to as a solder grid array or solder bump array. Ball grid arrays have solder studs arranged over the entire area of the lower face of the substrate, and these studs allow surface mounting on printed circuit boards or assemblies. The arrangement of the solder studs over the entire area allows a large number of connections to be provided in a coarse grid of, for example, 1.27 mm.

The use of what is referred to as MID technology, wherein MID means Molded Interconnection Devices, allows injection-molded parts with integrated conductor runs to be used rather than conventional printed circuits. High-quality thermoplastics which are suitable for injection molding of three-dimensional substrates are used as the basis for this technology. Thermoplastics such as these are characterized in comparison to conventional substrate materials for printed circuits by having better mechanical, chemical, electrical and environmental characteristics. In one specific direction of MID

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technology, referred to as SIL technology, wherein SIL is a German language abbreviation for "injection-molded parts with integrated conductor runs", a metal layer applied to the injection-molded parts is structured without any necessity for the otherwise normal mask technique by means of a

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special laser structuring process. In this case, a number of mechanical and electrical functions can be integrated in the three-dimensional injection-molded parts with a structured metallization. The package support functions are carried out at the same time by guides and snap-action connections, while the metallization layer is used for electromagnetic shielding in addition to the wiring and connection function, and the metallization layer ensures good heat dissipation. Appropriate plated-through holes are produced during the injection-molding process itself in order to provide electrically conductive cross-connections between two wiring systems on mutually opposite surfaces of the injection-molded parts. The inner walls of these plated-through holes are then likewise coated with a metal layer, during the metallization of the injection-molded parts. Further details relating to the production of the three-dimensional injection-molded parts with integrated conductor runs can be found, for example, in DE-A-37 32 249 or in EP-A-0 361 192.

A single-chip module is known from WO-A-89/00346, in which the injection-molded, three-dimensional substrate is composed of an electrically insulating polymer and, on its lower face, has studs which are formed at the same time during the injection-molding process and which studs can also be arranged over the entire surface, if required. An IC chip is arranged on the upper face of this substrate, and its connections are connected via fine bonding wires to interconnects formed on the upper face of the substrate. These interconnects are themselves connected via plated-through holes to associated external connections formed on the studs.

What is referred to as a polymer stud grid array (PSGA) is known from WO-A-96/09646, and this combines the advantages of a ball grid array (BGA) with the advantages of MID technology. The use of the expression

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polymer stud grid array (PSGA) for the new type is based on the expression ball grid array (BGA), with the expression "polymer stud" being intended to indicate polymer studs that are formed at the same time as the injection molding of the substrate. The

new type, which is suitable for either single-chip, few-chip or multi-chip modules, has

- an injection-molded, three-dimensional substrate composed of an electrically insulating polymer,
- polymer studs which are arranged over the entire area and are formed at the same time during the injection-molding process on the lower face of the substrate,
- external connections formed on the polymer studs by means of a detachable end surface,
- conductor runs which are formed at least on the lower face of the substrate and connect the external connections to the internal connections, and
- at least one chip which is arranged on the substrate and whose connections are electrically ~~conductively~~ connected to the internal connections.

In addition to the simple and cost-effective production of the polymer studs during the injection-molding process for the substrate, the external connections on the polymer studs can also be produced with minimal effort, together with the normal production of the conductor runs as for MID technology or SIL technology. The fine laser structuring, which is preferred for SIL technology, allows the large numbers of connections to be provided on the polymer studs, in a fine grid.

Another preferable factor is that the thermal expansion of the polymer studs corresponds to the thermal expansions of the substrate and of the wiring that holds the module. This results in highly reliable soldered connections even when temperature fluctuations occur frequently.

It is also known, from US-A-5 477 087, for the elastic characteristics and the temperature response of the polymer

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studs to be utilized for making contact with electronic components, such as semiconductors. To this end, a metal barrier layer is first of all in each case applied to the aluminum electrodes of the electronic components, ~~with~~ and the

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polymer studs are then ~~being~~ formed on these metal layers. The completely formed polymer studs are then coated with a layer of a metal which has a low melting point.

If polymer stud grid arrays or other components with metallized polymer studs are connected to wiring systems such as printed circuit boards, for example, by means of reflow soldering, then there is a risk of the molten solder being drawn upward along the metallization on the polymer studs. This phenomenon, which occurs with about 75% of the polymer studs, then, however, itself leads to nonreproducible solder layer thicknesses under the polymer studs and, possibly, to short circuits, to adjacent interconnects.

Summary of the Invention

The invention ~~specified in claim 1~~ is based on the problem of ensuring reproducible solder layer thicknesses under the polymer studs in the case of a substrate having polymer studs for soldered connections to a wiring system.

forms a step or steps which

The invention is based on the knowledge that a polymer stud geometry having at least one projection makes it possible to prevent the ~~mold on the~~ molten solder from being drawn upward ~~by means of the step or steps formed in this way~~. This results in reproducible solder layer thicknesses under the polymer studs which, for their part, ensure highly reliable soldered connections. The risk of short circuits which are caused by solder being drawn upward can likewise be prevented.

~~Advantageous refinements of the invention are specified in the dependent claims.~~

of the stud is for its projection to be a conical, cylindrical Projection,

The refinement ~~as claimed in claim 2, is particularly~~ which is suitable for production of substrates with integral polymer studs by means of injection molding. In this

MARKED-UP VERSION

- 4a -

case, the dimensions ~~specified in claim 3 for the cylindrical projections~~ of a cylindrical projection of a diameter between 100 and 250 µm and a height of between 25 and 300 µm

in a polymer stud grid arrays have led to particularly reliable soldered connections.

Insert A from page 5a

The variants for the geometry of the polymer studs ~~specified in claims 4, 5 and 6 likewise prevent the~~ solder from being drawn upward, by means of the steps. This results in the capability to match the geometry of the polymer studs to particular applications.

Exemplary embodiments of the invention are described in more detail in the following text and are illustrated in the drawing, ~~in which:~~

Brief Description of the Drawings

Figure 1 shows a section, illustrated in cutaway form, through a substrate having integrally formed, stepped polymer studs,

Figure 2 shows a cross section of a polymer stud on the substrate shown in Figure 1, with a metallization applied to it and with a conductor run leading away from the polymer stud,

Figure 3 shows a cross section of a soldered connection of the polymer stud illustrated in Figure 2 to a wiring system,

Figure 4 shows a cross section of a first variant ~~with~~ of a polymer stud having ~~two studs~~ a compound projection,

Figure 5 shows a cross section of a second variant for the polymer studs, with a number of projections arranged on one step, and

Figure 6 shows a cross section of a third variant for the polymer studs, with an annular projection.

Description of the preferred embodiments

Figure 1 shows a section through a substrate S, on whose lower face U polymer studs PS, which are also

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formed during the injection molding of the substrate, are arranged in order to form a

Insert A

, which include a projection with a second projection extending therefrom ~~Two projections to each~~ a number of projections, and an annular projection on the stop, also prevent Two steps,

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polymer stud grid array. As can be seen, the slightly conical polymer studs PS are each provided at their lower end with cylindrical projections E. The diameters of the cylindrical projections E are of such a size that an annular step ST is in each case formed as the transition to the rest of the polymer stud PS. In the illustrated exemplary embodiment, a polymer stud PS has a diameter D of 400 µm in its base region, while the height H, as the distance between the lower face U of the substrate S and the step ST, is 400 µm. The diameter d of the cylindrical projection E is 160 µm, while the height h of the cylindrical projection E is 50 µm.

Figure 2 shows a polymer stud PS as shown in Figure 1 after a very-fine laser structuring of a metal layer which is applied to the entire surface of the substrate S. As can be seen, the polymer stud PS, including the cylindrical projection E, is provided with a metallization M, and a conductor run LZ leads away from the polymer stud PS on the lower face U of the substrate S.

Figure 3 shows the soldered connection of the polymer stud PS, illustrated in Figure 2, to a wiring system V which, in the illustrated exemplary embodiment, is in the form of a printed circuit board LP with connecting pads AP arranged on the upper face. This clearly shows that all the solder L remains in the area between the step ST and the connecting pad AP during reflow soldering, and is not drawn up ~~as far as~~ along the sides of the stud towards the conductor runs LZ ~~at the sides~~, as in the case of polymer studs without a step. The geometry of the stepped polymer studs PS thus ensures reproducible layer thicknesses for the solder L.

In the first variant illustrated in Figure 4, ~~the~~ a polymer stud PS ~~which are~~ integrally formed on a

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substrate S1, ~~are annotated PS~~/ A double step on the polymer studs PS1 results in an annular projection E1 and a cylindrical

projection E10 being formed. ~~The associated annular steps are annotated~~ ST1 and ST10 ~~respectively~~.

In the second variant, which is illustrated in Figure 5, the polymer studs ~~which~~ are integrally formed on a substrate S2. ~~are annotated PS2~~. A total of four cylindrical projections E2, which are arranged spaced apart from one another, are provided on a step ST2 in the form of a platform.

In the third variant, which is illustrated in Figure 6, the polymer studs ~~which~~ are integrally formed on a substrate S3 ~~are annotated PS3~~. An annular projection E3 is in this case located on a step ST3, which is likewise in the form of a platform.

Apart from the slightly truncated conical polymer studs illustrated in Figures 1 to 6, polymer studs or projections with other cross-sectional shapes may also be used. However, the formation of at least one step which prevents the solder from being drawn up at the sides during reflow soldering is also of critical importance ~~here~~.

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~~Patent Claims~~
I claim:

(amended) 1. A substrate [(S; S1; S2; S3)] having at least two metallized polymer studs [(PS; PS1; PS2; PS3)] for soldered connections to a wiring [(V)] and having conductor runs [(LZ)] which lead away from the polymer studs [(PS; PS1; PS2; PS3)] on [the] a lower face [(U)] of the substrate [(S; S1; S2; S3), with] each [the] polymer studs [(PS; PS1; PS2; PS3)] having at least one step [(ST; ST1, ST10; ST2; ST3)] in order to form at least one projection [(E; E1; E10; E2; E3)].

(amended) 2. The substrate [(S)] as claimed in according to claim 1, [characterized by] wherein the projection is a cylindrical projection [(E)] which is arranged concentrically with respect to the polymer stud [(PS)].

(amended) 3. The substrate [(S)] as claimed in according to claim 2, [characterized in that] wherein the cylindrical projection [(E)] has a diameter [(d)] of between 100 µm and 300 µm, and a height [(h)] of between 25 µm and 250 µm.

(amended) 4. The substrate [(S1)] as claimed in according to claim 1, [characterized in that] wherein the polymer studs [(PS1)] are provided [having] with two projections [(E1; E10)] and two steps [(ST1; ST10)].

(amended) 5. The substrate [(S2)] as claimed in according to claim 1, [characterized in that] wherein each of the polymer studs [(PS2)] are provided [having] with a number of projections [(E2)] arranged at a distance from one another on [a] the step [(ST2)].

(amended) 6. The substrate [(S3)] as claimed in according to claim 1, [characterized in that] wherein each of the polymer studs [(PS3)] are provided [having] with annular [projections (E3)] projection arranged on [a] the step [(ST3)].

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Abstract of the disclosure

~~Substrate having at least two metallized polymer studs for soldered connections to wiring~~

A substrate (S) having at least two metallized polymer studs (PS), in particular a polymer stud grid array, is designed ~~such~~ so that the polymer studs (PS) have at least one step (ST) and at least one projection (E) extending from the step. This geometry of the solder studs (PS) ensures reliable soldered connections to a wiring (W) and reproducible layer thicknesses of the solder (L).

~~Figure 3~~

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